REMARKS

Claims 1-10 and 12-20 are pending in this application. Claims 1, 4, 6-8, and 10 are amended herein. Claims 12-20 have been added. Claim 11 has been canceled herein. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

The disclosure was objected to for an incorrect or missing reference numbers. The reference numbers have been corrected and/or added, and therefore the objection to the specification is now moot.

Claim 10 was rejected under 35 U.S.C. 112 as being indefinite. Claim 10 has been amended to clear up any indefinition.

Claim 11 was rejected under 35 U.S.C. 102(e) as being anticipated by Lee. However, claim 11 has been canceled.

Claims 1-8 and 10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Funaba, *et al.* in view of Lee, and claim 9 was rejected under 35 U.S.C. 103(a) as being unpatentable over Funaba, *et al.* in view of Lee and in further view of Angelucci.

However, all of the claims have been amended and two new independent claims added that clearly patentably define over all of the references of record, whether considered singly or in combination. As an example, claim 1 has been amended and new independent claim 14 is written to define that a first signal bus portion *on the circuit board* is connected to the first slot connector or means for receiving and that the second signal bus portion *on the circuit board* is connected to the second means for receiving or slot connector and not connected to the first signal bus portion. The first memory module and the second memory modules connected via the flexible bridge are received in the first and second slot connectors or means for receiving, so that

the first and second memory modules are serially-connected between the first and second signal bus portions.

Neither Lee nor Funaba, *et al.* teaches memory modules serially-connected between bus portions on a circuit board. Thus, a person skilled in the art, combining Lee and Funaba, *et al.*, would not obtain what is claimed in the suggested independent claim 1. Moreover, there is no hint in either of the references that would motivate a person skilled in the art to combine the teachings of Lee and Funaba, *et al.*

Therefore, it is respectfully submitted that the subject matter of claim 1 is not suggested by the prior art.

Although neither Funaba, *et al.* nor Lee teach the use of signal bus portions as taught and claimed in the present invention, Funaba, *et al.* does teach various methods for serially-connecting a number of memory modules, as shown in FIGs. 1, 10, 13, and 31A, for example. Therefore, Funaba, *et al.* itself provides a person skilled in the art with a number of possibilities as to how serially-connected memory modules can be implemented, but still did not come up with the advantageous method described in the present invention. Further, there is no hint in the prior art that would motivate a person skilled in the art to deviate from the approaches taught by Funaba, *et al.* by making use of a flexible bridge, as taught by Lee.

In addition, as can be derived from FIGs. 1and 2 of the present application, the flexible bridges are preferably designed such that the respective pair of memory modules can be used according to FIGs. 1 and 2. To this end, the flexible bridge and, thus, the signal lines thereof have to be provided with a sufficient length. This is clearly not the case with the flexible bridge taught by Lee.

In addition, both new independent claims 14 and 20 now clearly require slot connectors that receive only a single memory module when FIGs. 1-10 and 50 of Funaba, *et al.* clearly shows that except for the end pieces, the receiving means of Funaba, *et al.* can connect to two different memory modules. FIGs. 11-14 and 45-48 of Funaba, *et al.* do show connectors receiving a single memory module, but use other techniques to connect the modules in series or are not concerned about such a series connection.

In any event, new independent claim 20 also includes a combination of elements not believed to be suggested by the references of record.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone James C. Kesterson, Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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